



KSZ9021 Errata Sheet

The following errata apply to the following products (silicon revisions):

- KSZ9021RL (rev-A2)
- KSZ9021RN (rev-A2)
- KSZ9021GN (rev-A2, A3)
- KSZ9021GQ (rev-A2, A3)

Item #	Erratum (description of problem)	Solution / Workaround
1	When two KSZ9021 PHYs are link partners and have auto MDI/MDI-X enabled, the link up time can take nearly 10+ seconds for <10% of the link up attempts. This applies to 1000Base-T link-ups only.	Need to wait for link up if auto MDI/MDI-X is enabled. or Disable auto MDI/MDI-X.
2	When KSZ9021 is in Forced 10/100Mbps mode (auto-negotiation disabled), auto MDI/MDI-X is automatically disabled by the KSZ9021 to help resolve long link up time with a link partner that has both auto-negotiation and auto MDI/MDI-X enabled.	Need to program register 1Ch bit [7] to set the RJ-45 pairs (1,2) and (3,6) to either MDI mode or MDI-X mode if link partner has auto MDI/MDI-X disabled. Note – register 1Ch bit [6] for auto MDI/MDI-X enable/disable is automatically disabled by the KSZ9021 in forced 10/100 Mbps mode, and can not be re-enabled when the KSZ9021 is still in Forced 10/100 Mbps mode.
3	KSZ9021 fails to link up after register 4h bit [11] (Asymmetrical Pause) is set.	Do not enable (set to 1) register 4h bit [11] for Asymmetric PAUSE support. or Disconnect and re-connect cable after setting register 4h bit [11] to 1.
4	PHY Address 0 is not supported.	Use the following PHY Addresses instead: <ul style="list-style-type: none">▪ 1 to 7 : for KSZ9021RL/RN/GN▪ 1 to 31 : for KSZ9021GQ
5	The 125MHz reference clock (CLK125_NDO pin) output has duty cycle variation when the KSZ9021 links up in 1000Base-T Slave mode, resulting in wide variation on the falling clock edge.	Use only rising edge of CLK125_NDO output for PLL locking. or Set KSZ9021 to always link up in 1000Base-T Master mode by setting register 9h bits [12:11] to '11'.

For any questions about this errata and sample request, please contact your Micrel FAE or local Sales Representative.